VOLTAGE LEVEL SHIFTER

BACKGROUND

[01] In order to perform read, program and erase operations in Flash memory, it is generally necessary to apply high voltages (higher than the typical control logic VCC supply) to the Flash cell. However, consumers are demanding higher speeds and lower power consumption. Higher speeds, of course, typically require faster transistors. One technique for designing and manufacturing faster transistors may be to decrease the distance between the transistor gate and the drain. However, this may create a high voltage overstress problem. As the distance between the gate and the drain diffusion decreases the maximum operating voltage of the transistor may decrease. If the distance is too small the silicon barrier between the gate and drain may have an excessive leakage current or may break down completely. Conversely, if the power supply voltage is lowered then the transistors may be made smaller and faster.

[02] Also, if the operating voltage is decreased by some factor but the current drawn by the transistor does not increase by more than that factor, then the power consumption may decrease or at least not increase.

[03] Therefore, making smaller transistors generally results in faster transistors and reduced power consumption. However, a Flash memory typically requires a high voltage to program, read and erase the Flash memory cell. Therefore, a level shifter circuit may be used to interface between the low voltage requirements of the control circuitry and the high voltage requirements of the Flash memory cell.

[04] A level shifter typically takes a low voltage input, usually a logical voltage, and level shifts it to a high voltage. Two primary types of level shifters are currently in use. The traditional level shifter uses a cross-coupled P-devices formation. This type of level shifter is typically the fastest and consumes the least power. A ratioed logic level shifter is smaller but consumes more power than the traditional level shifter.

[05] However, a problem may arise when using conventional level shifters between the low voltage, fast transistor logic circuitry and a high voltage Flash memory: the level shifters are in the control path for the Flash memory and, if made entirely of high voltage devices, may be

slower. This adversely impacts the memory read, write and erase times, and therefore may adversely impact product performance.

BRIEF DESCRIPTION OF THE DRAWING

[06] The Figure is a schematic diagram of an embodiment of the present invention.

DETAILED DESCRIPTION

[07] Turn now to the figure, which is a schematic diagram of an exemplary embodiment of the present invention. An exemplary environment of the present invention is in conjunction with a Flash memory device 7 having low-voltage, high speed logic circuits 5 and Flash-type memory cells 6. However, the present invention may be used in conjunction with low-voltage circuits and high-voltage circuits in general. In the exemplary environment, the exemplary embodiment may be internal to a Flash memory device 7 and may be interposed between a low voltage, high speed logic control circuit 5 and one or more Flash memory cells 6. The control circuit 5 may read and/or may write to the memory cell 6 and, as such, typically may comprise a high speed decoding circuit, which may include, for example, a microprocessor. Whereas the logic circuit 5 generally requires a "low" operating voltage of 1 to 5 volts, depending upon the technology, the Flash memory 6 typically requires a "high" operating voltage, typically 8 to 11 volts, and even higher voltages, e.g., 20 volts, for some technologies.

[08] A Flash memory device 7 may comprise a plurality of Flash memory cells 6, arranged in rows and columns. A particular cell may be selected by activating a row control line and a column control line. Typically, a plurality of cells may be associated to form a logical word, which may be of any convenient length, 16 bits, 32 bits, 64 bits, etc. The logical word may then be accessed by activating the row control line for that word, and activating all of the column lines. A row control line is often referred to as a wordline.

[09] In the exemplary environment the Flash memory device 7 may have a plurality of words and wordlines and, therefore, a plurality of the level shifter circuit 1 may be used, one for each wordline.

[10] The circuit 5 may provide a plurality of output signals VIN-A through VIN-N which may be used to select the particular wordline 16. Signals VIN-A through VIN-N may be connected to the gates of N-type transistors 12A – 12N, respectively. Transistors 12A – 12N may be low to ultra-low voltage, high speed transistors, and may be connected in series. Interposed between the drain of transistor 12A and the operating supply voltage VPP may be the series combination of a P-channel metal oxide semiconductor (P-type) transistor 10 and an N-channel metal oxide semiconductor (N-type) transistor 11. The signal VREF may be connected to the gate of transistor 10 so as to weakly bias it on. Transistor 10 may therefore function as, or may be considered to be, a weak or limited constant current source, or a current-limiting resistor. The signal VBIAS may be used to control the operation of transistor 11 and may also serve to assist in providing the benefits described herein. Transistor 11 may be used in a source-follower mode of operation but its pull-up capability may be limited by the limited current supplied by transistor 10. Transistors 10, 11, 14 and 15 may be high voltage, high speed transistors.

[11] Consider first the situation where all the signals VIN-A through VIN-N are a logical one or "on". All of transistors 12A – 12N may be turned on. Due to the limited current available from transistor 10, transistor 11 may not be able to source enough current to maintain the voltage at node 22A, so the voltages at nodes 22A – 22N may be low. As the voltage at node 22A may be low, and the current-sourcing capability of transistor 10 may be limited, transistor 11 may pull down the output of transistor 10, so the voltage at node 21 may be low.

[12] Node 21 may be connected to the gates of the series combination of P-type transistor 14 and N-type transistor 15, which may function as an inverter or inverting driver. The source of transistor 14 may be connected to VPP, the source of transistor 15 may be connected to circuit ground, and the drain of transistor 14 and the drain of transistor 15 may be connected together and to the VOUT output signal line 16. Thus, when node 21 is low, transistor 14 may be turned on, transistor 15 may be turned off, and the VOUT output signal line 16 may be pulled to VPP by transistor 14, thereby selecting that word line 16.

[13] Consider now the situation where at least one of the signals VIN-A through VIN-N may be a logical zero or "off". For convenience of discussion, assume that signal VIN-A may be off,

and the other VIN signals may be on. Transistor 12A may be off, so the series combination of transistors 12A – 12N may represent an open circuit, and may not sink any current. Thus, if transistor 11 were not present (i.e., replaced by a source-drain short) then transistor 10 may pull nodes 21 and 22A up to VPP, and the full high voltage VPP may be impressed across transistor 12A. If transistor 12A is a low-voltage device, then it may be destroyed. Therefore, without transistor 11, transistors 12A – 12N may have to be high-voltage devices, which may require them to be slower, larger, higher-power and/or more expensive devices. Further, these high-voltage transistors may, as a consequence, have a higher turn-on threshold voltage (Vt) which may approach or even exceed the maximum output voltage of some ultra-low voltage technologies. As Vt may vary depending upon the process and upon the operating temperature, the operation of these high-voltage transistors may become slow, erratic, or even non-functional.

[14] However, if transistor 11 is present, and is used in a source-follower mode, then the node 22A may only be allowed to rise to VBIAS – VT11, where VT11 is the gate-source turn-on voltage of transistor 11. Thus, the maximum voltage that may be impressed across transistor 12A is VBIAS – VT11. Therefore, transistors 12A – 12N may be low-voltage devices, and therefore may be smaller, faster, lower-power and/or less expensive devices without sacrificing speed. As a result of at least one transistors 12A – 12N being off, transistor 10 may pull node 21 to VPP, thereby turning off transistor 14, and turning on transistor 15, which may cause the VOUT output signal line 16 to be low, thereby deselecting that word line 16.

[15] VPP may be provided from a selectable voltage power supply and may vary from zero volts to 12 volts, VBIAS may be 2 volts, VREF may be zero volts, VIN-A through VIN-N may be zero to 1 volt (logic signals), the voltage at node 21 may vary from zero volts to VPP, and the voltage at nodes 22A – 22N may vary from zero volts to VBIAS-VT11. These voltages are not critical. Furthermore, if a negative supply voltage (VSS) is used rather than circuit ground, then the lower voltages may change accordingly, e.g., the voltage at node 21 may vary from VSS to VPP.

[16] In theory, the metal oxide semiconductor (MOS) transistors 11, 12A-12N, 14 and 15 may require no drive current and the current provided by transistor 10 may be extremely small

or even zero. However, in actual practice, transistors may have leakage currents. Therefore, the current provided by transistor 10 must be at least sufficient to turn on transistor 15 and turn off transistor 14. Further, there may be a capacitance associated with the gate of transistors 14 and 15, so the current provided by transistor 10 must also be at least sufficient to charge or discharge these capacitances quickly enough to achieve the desired switching speed. Similarly, transistors 11 and 12A-12N must be able to sink enough of the current from transistor 10 to turn on transistor 14 and turn off transistor 15. Further, because of the capacitance mentioned above and associated with the gate of transistors 14 and 15, the current sunk by transistors 11 and 12A-12N must also be at least sufficient to charge or discharge these capacitances quickly enough to achieve the desired switching speed. However, the larger the current provided by transistor 10, the larger the power consumption, so the maximum current provided by transistor 10 is a design choice.

[17] Although the exemplary environment is in a Flash memory, the present invention is not so limited and may be used in any situation where a voltage-level shifting circuit using lower-voltage devices is desired or required. For example, an embodiment may be used for voltage-level shifting between different technologies or where it is desired to interface two devices which operate under different standards. Also, although the exemplary embodiment contemplates two or more input signals VIN and, therefore, a corresponding number of transistors 12, an embodiment may also be used where there is only one input signal VIN-A and one corresponding transistor 12A. In addition, the use of transistors 14 and/or 15 may not be necessary in some situations, and the signal at node 21 may be used as the output signal. Further, although transistors 14 and 15 have been described in an inverting configuration, they may also be connected in a non-inverting configuration. Finally, although semiconductor devices 10, 11, 12, 14 and 15 have been described herein as P-channel or N-channel metal oxide semiconductors, other semiconductor types, although possibly less favored because of power consumption, heat generation, size, and other factors, may also be used, for example, bipolar transistors.

[18] While an exemplary embodiment and its exemplary environment have been described above and shown in the accompanying drawing, the present invention is not so limited as

various modifications may occur to those of ordinary skill in the art upon reading this disclosure. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.